BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

B7

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 December 2002 (27.12.2002)

PCT

(10) International Publication Number
WO 02/103760 A2

(51) International Patent Classification[7]: H01L 21/00

(21) International Application Number: PCT/US02/18973

(22) International Filing Date: 14 June 2002 (14.06.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/298,153 14 June 2001 (14.06.2001) US

(71) Applicant: AMBERWARE SYSTEMS CORPORATION [US/US]; 13 Garabedian Drive, Salem, NH 03079 (US).

(72) Inventors: HAMMOND, Richard; 16 St. Paul Street, Apt. 1, Cambridge, MA 02139 (US). CURRIE, Matthew; 36 Symphony Road, Apt. 1A, Boston, MA 02115 (US).

(74) Agents: CONNORS, Matthew, E. et al.; Samuels, Gauthier & Stevens, LLP, Suite 3300, 225 Franklin Street, Boston, MA 02110 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 02/103760 A2

(54) Title: METHOD OF SELECTIVE REMOVAL OF SIGE ALLOYS

(57) Abstract: A method is disclosed of forming buried channel devices and surface channel devices on a heterostructure semiconductor substrate. In an embodiment, the method includes the steps of providing a structure including a first layer having a first oxidation rate disposed over a second layer having a second oxidation rate wherein the first oxidation rate is greater than the second oxidation rate, reacting said first layer to form a sacrificial layer, and removing said sacrificial layer to expose said second layer.

METHOD OF SELECTIVE REMOVAL OF SiGe ALLOYS

The present application claims priority to U.S. Provisional Patent Application Ser. No. 60/298,153 filed June 14, 2001, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

The present invention generally relates to the fabrication of semiconductor substrates from devices, and in particular relates to the use of strained silicon (Si) heterostructure substrates in forming devices such as transistors, for example, for high-performance CMOS integrated circuit products.

As microelectronic systems require faster operating speeds and increased computing power, the need exists for integrated circuits to provide a greater complexity of transistors in a smaller amount of circuit real estate. Such integrated circuits include, for example, microprocessors, ASICs, embedded controllers, and millions of transistors, such as metal oxide silicon semiconductor field-effect transistors (MOSFETs).

Certain microelectronics systems, such as radars, satellites, and cell phones, require low-power, high-speed, and high-density circuits with a high signal-to-noise ratio (i.e., low noise). These low power, high speed, and low noise requirements present a significant design challenge both at the circuit design and at the transistor design level. Microelectronic devices that include both analog and digital circuits are used together to achieve these requirements. Analog devices are used in applications requiring high speed and low noise, whereas digital circuits are used in applications requiring high density and low power.

Microelectronic devices that include both analog and digital circuits on the same substrate typically use traditional Si based MOSFET devices. Analog MOSFET devices, which run on analog signals, typically exhibit noise problems because noise is induced at high frequency when carriers scatter along the Si/SiO_2 interface of a traditional MOSFET device. Thus, for high-speed analog devices, field-effect transistors (FETs) are not used; rather, bipolar transistors that do not have conduction along a Si/SiO_2 interface are used. Unfortunately, it is difficult and expensive to integrate both bipolar and MOSFET devices on a single substrate.

One way to reduce noise and to achieve devices that are integrated on the same substrate is through changes at the transistor design level by using surface channel devices along with buried channel devices. A conventional Si based buried channel FET device has a channel conduction layer that is buried within a highly doped silicon region. This buried channel device has low noise because the charge carriers in the conduction channel are spatially separated from the Si/SiO_2 interface.

While it is possible to build surface channel devices and buried channel devices on the same substrate, the manufacturing process requires complex and extensive process capabilities. For example, use of ion implantation to populate the buried channel requires counterdoping of the layers above the buried channel, and also requires extensive masking steps, adding to the cost and complexity of the overall manufacturing process. Furthermore, the excessive doping required to populate a buried conduction layer within a conventional silicon substrate places fundamental limitations on the performance of such a device.

Further, the use of strained semiconductor devices presents particular problems to the formation of surface channel devices and buried channel devices on the same substrate. For example, U.S. Patent No. 5,963,817 discloses a method of using local selective oxidation of bulk or strained SiGe for forming buried channel oxide regions involving steps of masking, oxidation (e.g., thermal oxidation), and oxide removal; and U.S. Patent No. 5,442,205 discloses the formation of surface channel semiconductor heterostructure devices with strained silicon device layers. It has been found, however, that the process of oxidation affects certain strained semiconductors differently. For example, the different layers of a strained semiconductor heterostructure may oxidize or become doped sufficiently differently that device formation procedures are compromised. Moreover, with high thermal budget oxidation, the thin strained semiconductor channels may be destroyed by significant interdiffusion during the high temperature oxidation steps.

There is a need, therefore, for a method of integrating surface channel and buried channel strained silicon devices on the same substrate

SUMMARY OF THE INVENTION

The invention provides a method of selectively removing SuGe alloy layers, thus exposing underlying semiconductor layers. The invention also provides a method of

forming buried channel devices and surface channel devices on a heterostructure semiconductor substrate. In an embodiment, the method includes the steps of providing a structure comprising a first layer having a first oxidation rate disposed over a second layer having a second oxidation rate, wherein the first oxidation rate is greater than the second oxidation rate, reacting said first layer to form a sacrificial layer, and removing said sacrificial layer to expose said second layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The following description may be further understood with reference to the accompanying drawing in which

Figures 1 - 9 show diagrammatic views of a heterostructure substrate during a method of providing buried and surface channel devices on the substrate in accordance with an embodiment of the invention;

Figure 10 shows the buried channel device and a surface channel device of Figure 9 coupled to a circuit; and

Figure 11 shows a diagrammatic graphical view of thermal oxidation time versus oxidation thickness for various semiconductor substrates.

The drawings are shown for illustrative purposes and are not to scale.

DETAILED DESCRIPTION OF THE INVENTION

The invention provides a simplified method of forming buried and surface channel heterostructure devices on the same substrate. As aforementioned, conventional Si based integrated buried and surface channel devices are typically manufactured using complex implantation procedures. In the present invention, the starting substrate material defines the buried and surface channel device structures. This starting material is a heterostructure where the the different materials in the heterostructure have different oxidation or removal properties. The difference in material properties allows for the selective removal of particular layers and this allows for the integration of varied device structures.

An exemplary embodiment of such a heterostructure substrate is a strained silicon substrate. A strained silicon (Si) substrate is generally formed by providing a relaxed SiGe layer on bulk Si through either epitaxial deposition or wafer bonding, and then providing a Si layer on the relaxed SiGe layer. Because SiGe has a different lattice

constant than Si, the Si layer becomes strained and results in enhanced mobilities (and hence improved device performance) compared with bulk Si. The percentage of Ge in the SiGe can have a dramatic effect on the characteristics of the strained Si layer.

In an embodiment, the invention involves the selective removal of SiGe alloys to form buried channel strained Si FET devices and surface channel strained Si FET devices on the same substrate. Using this method, both device types (e.g., digital and analog) may be realized on a common substrate and both have distinct advantages over conventional silicon MOSFET technologies. For example, a strained silicon surface channel device offers an enhanced drive current over a conventional Si based MOSFET due to its enhanced carrier mobilities. Similarly, the band offset of the strained silicon buried channel device offers low noise characteristics due to the spatial separation of the active charge carriers from both the SiO_2 interface and any remote impurity atoms introduced via ion implantation.

Figure 1 shows a diagrammatic cross-sectional view of a substrate 10, comprising a Si layer 12, a relaxed SiGe layer 14, a strained Si layer 16, a second SiGe layer 18, and a second strained Si layer 20. Each of the strained Si layers 16 and 18 may be between 50Å and 500Å. The substrate 10 forms an examplary base structure for the present invention. In developing this layered heterostructure substrate 10, epitaxial growth techniques (e.g., chemical vapor deposition) and polishing techniques (for example, chemical mechanical polishing) or wafer bonding techniques, which are known in the art, are applied. Methods of fabricating various strained silicon heterostructures are disclosed in U.S. Patent Application Ser. No. 09/906,551 filed July 16, 2001 and U.S. Patent Application Ser. No. 09/928,126 filed August 10, 2001, the disclosures of which are hereby incorporated by reference.

A variety of masking layers are then applied to the substrate of Figure 1 as shown in Figure 2. First, an oxide layer 22 is applied to the exposed strained silicon layer 20, followed by a nitride masking layer 24. A photoresist layer 26 is then applied to the nitride mask. Oxide masking layer 22 and nitride masking layer 24 are typically formed using low-pressure chemical vapor deposition (LPCVD), and are approximately 100Å and 500-1000Å thick, respectively. The photoresist layer 26 is typically a photosensitive polymer, such as a novolak-based photoresist, which is spun-applied. A chrome mask 28 is then utilized to expose selected regions of the photoresist layer 26 with ultraviolet light. The ultraviolet light exposes the uncovered regions of the photoresist layer 26.

This is followed by a developing step to remove the exposed regions of the photoresist layer 26.

As shown in Figure 3, after the exposed regions of the photoresist layer 26 are removed, the remaining regions of the photoresist masking layer 26 serve as a mask to etch the exposed regions of nitride masking region 24 and oxide masking region 22. The exposed regions of nitride masking layer 24 are removed by using a hot phosphoric acid, or CF_4/O_2 reactive ion etch (RIE), and the exposed regions of oxide masking layer 22 are removed using a HF acid etch step. The photoresist masking region 26 is then removed using a plasma O_2 ash. Note that a portion of strained Si cap layer 20 may possibly be removed in the process of removing the exposed region of oxide masking layer 22. The nitride masking region 24 then serves as a mask to etch the strained Si cap layer 20 in, for example, CF_4/O_2 RIE as shown in Figure 4. Note that this step may also etch into a portion of second SiGe layer 18.

The exposed portion of the second SiGe layer 18 is then selectively oxidized to expose the strained Si layer 16 leaving regions 32 of oxidized SiGe, for example, at or below approximately 850°C, and in some applications at or below approximately 700°C. The selective removal requires consideration of oxidation rates for Si and SiGe at various Ge concentrations. For example, Figure 11 shows that the selectivity of SiGe increases with an increase in concentration of Ge. For a 470 nm SiGe layer, the x-axis is the oxidation duration in hours and the y-axis is the square of the oxide thickness in $10^5 nm^2$. Line 1 represents the rate for a 36% Ge concentration in SiGe, line 2 represents a 28% Ge concentration in SiGe, and line 3 represents a 0% Ge concentration (i.e., pure Si). As the Ge concentration in SiGe increases, the oxidation rate increases for certain oxidation conditions. An example of oxidation conditions for which an acceptable oxidation rate differential occurs is oxidation at 700°C in a wet ambient. This indicates that oxidation of SiGe layer 18 will occur rapidly, and the oxidation step will slow down considerably as the oxidation front reaches the strained Si layer 16. Thus, the controlled selective removal of SiGe layer 18 takes advantage of this differential in oxidation rates. This differential may be further exploited by grading the second SiGe layer 18 such that the Ge concentration is higher at the intersection of second SiGe layer 18 and strained Si layer 16. This expedites the oxidation of second SiGe layer 18 at the intersection of second SiGe layer 18 and strained Si layer 16, thereby avoiding too much erosion of strained Si layer 16.

A differential chemical oxidation rate may also be exploited during a wet chemical processing step. For example, a standard RCA SC-1 clean ($NH_4OH+H_2O_2+H_2O$) may be used to preferentially remove the second SiGe layer 18 over the strained silicon layer 16. Again, this preferential chemical removal is due to the enhanced chemical oxidation rate of SiGe alloys compared to that of silicon.

A second nitride layer 30 is then formed using LPCVD (approximately 500-1000Å thick) over the entire surface of structure as shown in Figure 5. Note that the oxidized SiGe regions 32 of the SiGe layer 18 may undercut and extend partially underneath strained Si cap layer 20. Isolation trenches 34, 36 and 38 may then be formed to isolate the various regions from one another as shown in Figure 6. The devices may be isolated from one another as disclosed in U.S. Provisional Patent Application Ser. No. 60/296,976 filed June 8, 2001, the disclosure of which is hereby incorporated by reference.

The second nitride layer 30 and the remaining region of the nitride masking layer 24 are then removed via plasma CF_4/O_2 or hot phosphoric wet etch as shown in Figure 7. The oxide masking layer 22 and regions 32 of SiGe oxide are then wet etched using a buffered HF solution. This buffered HF solution etches oxide masking region 22 and SiGe oxide region 32, but stops on strained Si layer 16 and strained Si layer 20. In the same step, first isolation trenches 34, 36 and 38 are then planarized via etching to leave a relatively planar surface in both buried channel device region A and surface channel device region B as shown in Figure 8. A judicious choice of thickness for oxide masking layer 22 and an appropriate wet chemical etchant results in the degree of planarity required.

As shown in Figure 9, insulator layers 40 and 42 (of for example, SiO_2) are then applied to the substrate of Figure 8 via thermal oxidation of the strained Si layers 16 and 20. The first SiO_2 layer 40 and second SiO_2 layer 42 are the gate dielectric layers upon which buried channel and surface channel MOSFET devices 44 and 46 may be formed as shown in Figure 10. In other embodiments, a deposited gate dielectric (e.g., a high-k gate dielectric) layer may be used instead of the oxide layers 40 and 42. The buried channel device 44 and the surface channel device 46 each utilize the strained silicon layer 16 as the channel, and each may be coupled to a circuit as generally shown at 48 in Figure 10. Note that in this example, the devices are fabricated having doped source/drain regions, silicide regions, spacers, and isolation regions.

Although the invention has been shown in connection with a strained Si/SiGe heterostructure, those skilled in the art will appreciate that any heterostructure that allows for the selective removal of the layers overlaying the channel layer will also work. Additionally, instead of a strained Si channel layer, layers of SiGe, Ge or GaAs may be used, alternatively, a plurality of such layers may be used to optimize the transport characteristics. Furthermore, the selective removal of blanket SiGe alloy layers may also be employed during the fabrication of silicon-on-insulator (SOI) and strained silicon-on-insulator (SSOI) substrates.

Those skilled in the art will appreciate that numerous modifications and variations may be made to the above disclosed embodiments without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A method of forming a semiconductor substrate, comprising:

providing a structure comprising a first layer having a first oxidation rate disposed over a second layer having a second oxidation rate, wherein the first oxidation rate is greater than the second oxidation rate;

reacting said first layer to form a sacrificial layer; and

removing said sacrificial layer to expose said second layer.

2. The method as claimed in claim 1, wherein the second layer comprises a strained semiconductor.

3. The method as claimed in claim 1, wherein the second layer comprises Si.

4. The method as claimed in claim 1, wherein the first layer comprises Si or Ge.

5. The method as claimed in claim 1, wherein said semiconductor substrate further comprises a relaxed semiconductor layer disposed beneath said second layer.

6. The method as claimed in claim 5, wherein said relaxed semiconductor layer comrises Si or Ge.

7. The method as claimed in claim 1, wherein said semiconductor substrate further comprises an insulator layer disposed beneath said second layer.

8. The method as claimed in claim 7, wherein said insulator layer comprises silicon dioxide.

9. The method as claimed in claim 1, wherein said step of reacting said first layer to form a sacrificial layer comprises thermal oxidation.

10. The method as claimed in claim 9, wherein said thermal oxidation is performed at or below a temperature of approximately 850°C.

11. The method as claimed in claim 9, wherein said thermal oxidation is performed at a temperature at or below approximately 700°C.

12. The method as claimed in claim 1, wherein said step of reacting said first

layer to form a sacrificial layer comprises chemical oxidation

13. The method as claimed in claim 1, wherein said step of reacting said first layer to form a sacrificial layer is performed on a first region of said first layer and not on a second region of said first layer.

14. The method as claimed in claim 13, wherein said method further comprises forming a surface channel device in said first region.

15. The method as claimed in claim 13, wherein said method further comprises forming a buried channel device in said second region.

16. The method as claimed in claim 13, wherein said method further comprises:
forming a surface channel device in said first region; and
forming a buried channel device in said second region, wherein the channel of said surface channel device and said buried channel device comprises a second device layer.

17. The method as claimed in claim 16. wherein said second layer comprises Si and said first layer comprises SiGe.

18. The structure formed by the method of claim 1.

19. The structure formed by the method of claim 7.

20. The structure formed by the method of claim 16.

21. A method of forming devices on a substrate said method comprising the steps of:
providing a structure comprising a SiGe layer disposed over a strained semiconductor layer;
selectively removing said SiGe layer in a first region but not in a second region such that a surface channel device may be formed on said first region and a buried channel device may be formed on said second region.

22. A method of forming devices on a substrate, said method comprising the steps of:
providing a structure comprising a SiGe layer disposed over a strained semiconductor layer;

oxidizing said SiGe layer to form a SiGe oxide in a first region but not in a second region of said structure;

removing said SiGe oxide;

forming a surface channel device in said first region and a buried channel device in said second region such that the strained semiconductor layer serves as the channel layer of each device.

23. A structure comprising:

a strained semiconductor layer;

a surface channel device; and

a buried channel device, wherein said surface and buried channel devices include a channel comprising said strained semiconductor layer.

24. The structure as claimed in claim 23, wherein said strained semiconductor layer comprises Si.

25. The structure as claimed in claim 23, wherein said structure further includes a relaxed semiconductor layer.

26. The structure as claimed in claim 25, wherein said relaxed semiconductor layer comprises SiGe.

27. A circuit formed by interconnecting the buried channel device and the surface channel device of claim 23.

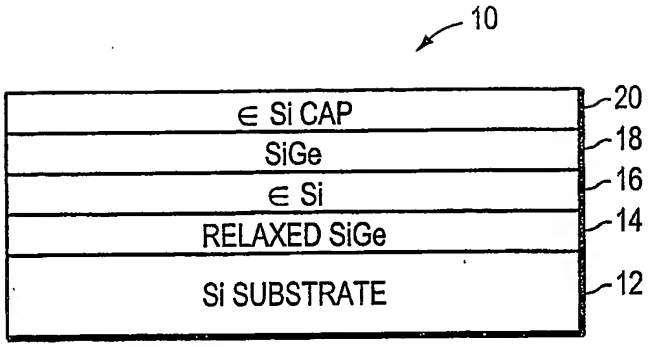
10
∈ Si CAP
SiGe
∈ Si
RELAXED SiGe
Si SUBSTRATE
20
18
16
14
12

FIG. 1

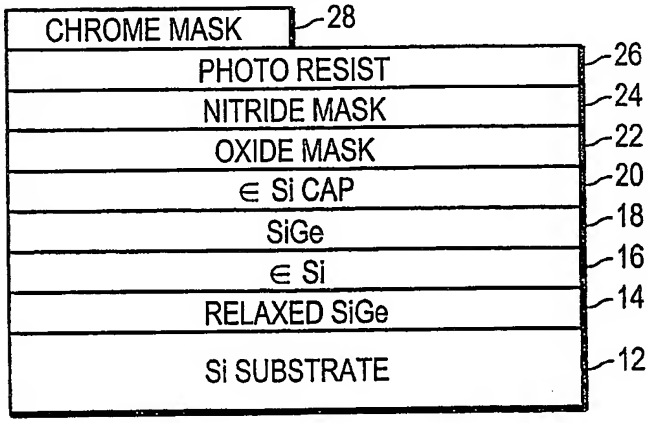
CHROME MASK
PHOTO RESIST
NITRIDE MASK
OXIDE MASK
∈ Si CAP
SiGe
∈ Si
RELAXED SiGe
Si SUBSTRATE
28
26
24
22
20
18
16
14
12

FIG. 2

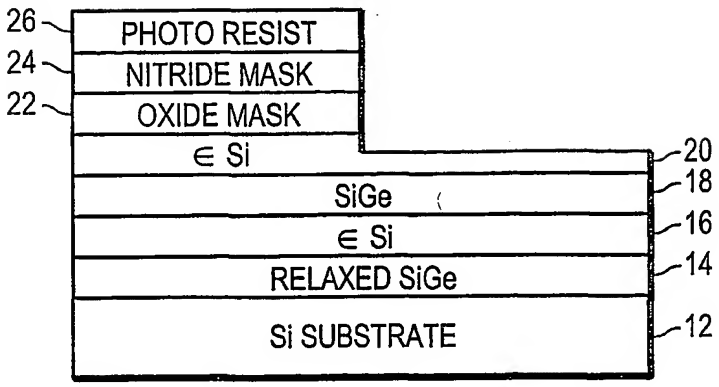
26
PHOTO RESIST
24
NITRIDE MASK
22
OXIDE MASK
∈ Si
20
SiGe
18
∈ Si
16
RELAXED SiGe
14
Si SUBSTRATE
12

FIG. 3

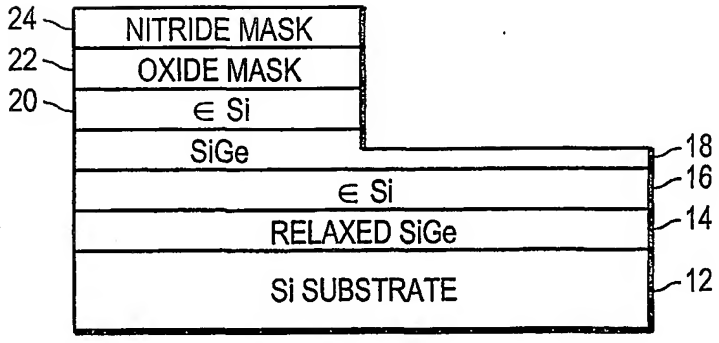
24
NITRIDE MASK
22
OXIDE MASK
20
∈ Si
SiGe
18
∈ Si
16
RELAXED SiGe
14
Si SUBSTRATE
12

FIG. 4

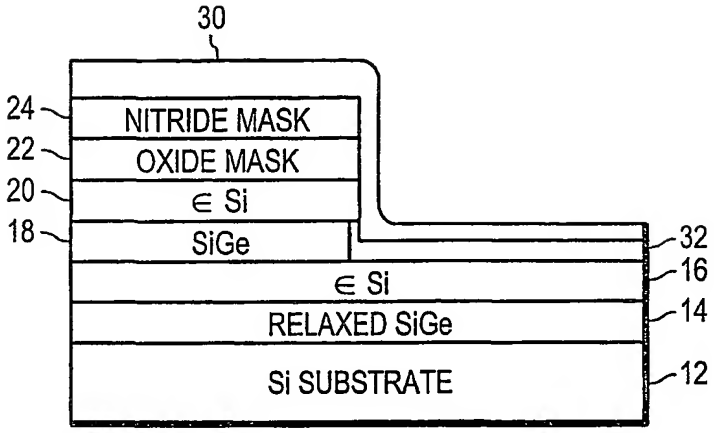
30
24
NITRIDE MASK
22
OXIDE MASK
20
∈ Si
18
SiGe
32
16
∈ Si
14
RELAXED SiGe
12
Si SUBSTRATE

FIG. 5

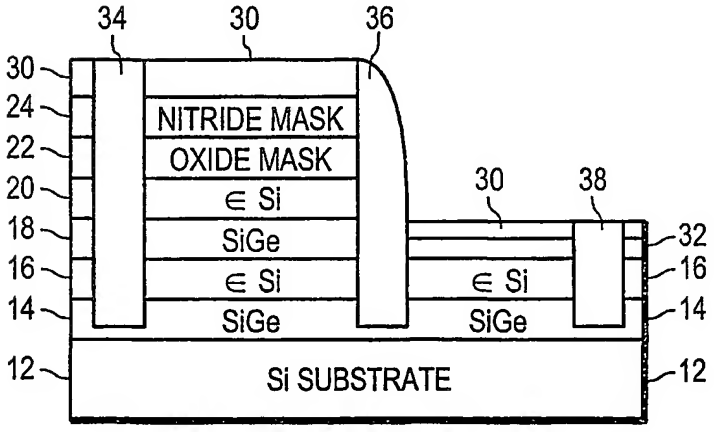
34
30
36
30
24
NITRIDE MASK
22
OXIDE MASK
20
∈ Si
30
38
18
SiGe
32
16
∈ Si
∈ Si
14
SiGe
SiGe
14
12
Si SUBSTRATE
12

FIG. 6

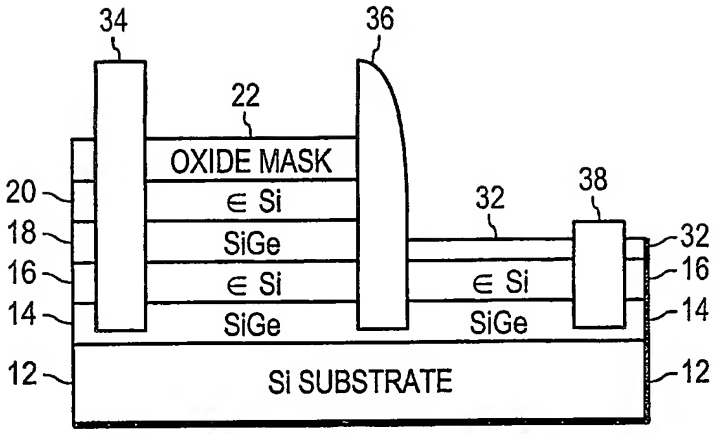
34
36
22
OXIDE MASK
∈ Si
SiGe
∈ Si
SiGe
20
18
16
14
12
32
38
32
16
14
12
∈ Si
SiGe
Si SUBSTRATE

FIG. 7

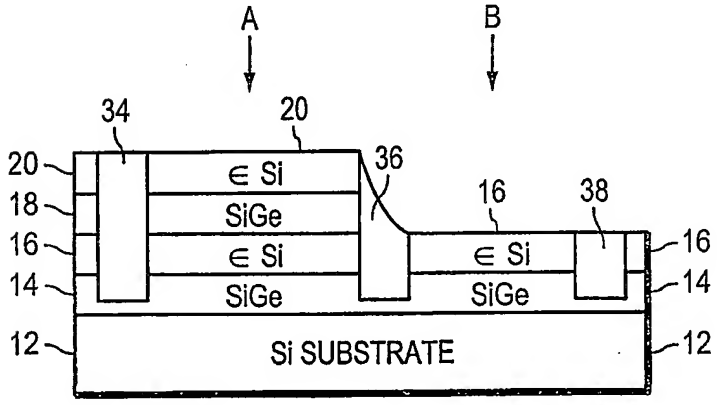
A
B
34
20
36
16
38
20
18
16
14
12
∈ Si
SiGe
∈ Si
SiGe
16
14
12
Si SUBSTRATE

FIG. 8

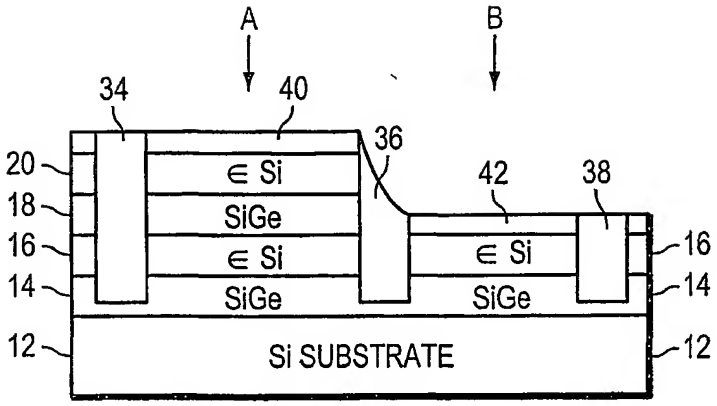
A
B
34
40
36
42
38
20
18
16
14
12
∈ Si
SiGe
∈ Si
SiGe
∈ Si
SiGe
Si SUBSTRATE

FIG. 9

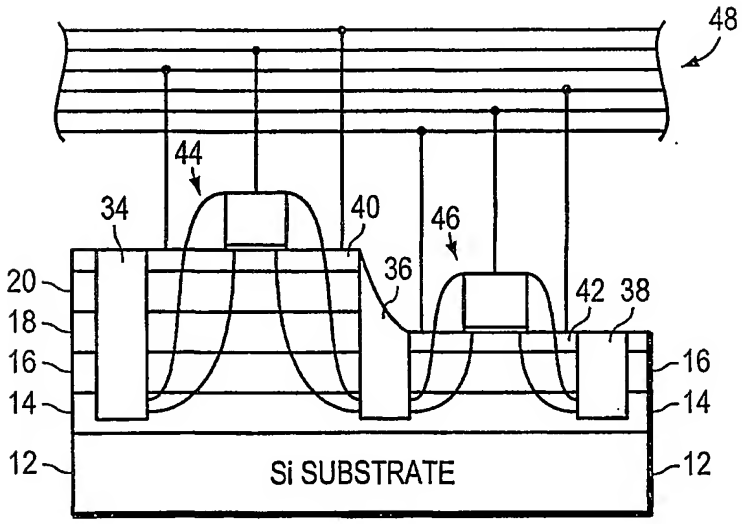
48
44
34
40
46
36
42
38
20
18
16
14
12
Si SUBSTRATE

FIG. 10

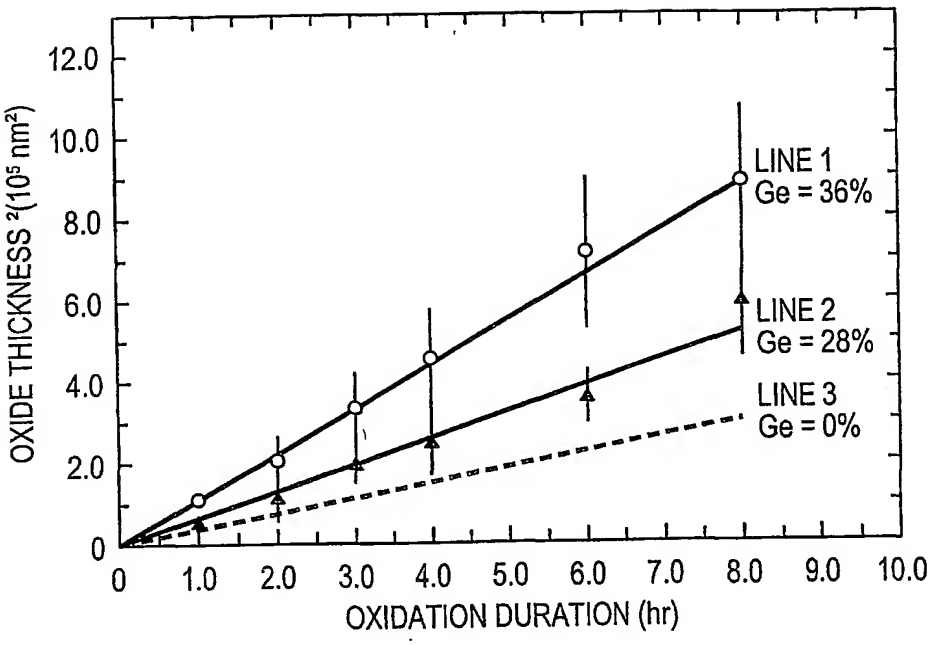
12.0
10.0
8.0
6.0
4.0
2.0
0
OXIDE THICKNESS ²(10⁵ nm²)
0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
OXIDATION DURATION (hr)
LINE 1
Ge = 36%
LINE 2
Ge = 28%
LINE 3
Ge = 0%

FIG. 11